# EXHIBIT J

# A HIGHLY RELIABLE 16 OUTPUT HIGH VOLTAGE NMOS/CMOS LOGIC IC WITH SHIELDED SOURCE STRUCTURE

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## ABSTRACT

A high voltage MOS IC, which consists of 16 high voltage NMOS transistor array having 400 V, 0.5 A output characteristic and its control CMOS logic, was newly developed. High and low voltage NMOS transistors of the IC are equipped with shielded source structure to realize completely parasitic bipolar effect-free high voltage MOS ICs.

Practically, this IC successfully drove a plasma display panel at 200 V, 2 MHz without any parasitic effect and its high operation reliability was verified.

To examine high integration density possibility, parasitic bipolar effects due to the interferences between high and high voltage transistors, low and low voltage transistors, and high and low voltage transistors, were experimentally investigated. As a result, it was confirmed that the "shielded source structure" realizes high density high voltage MOS ICs.

## INTRODUCTION

Recently, the cost and size reduction, and display area enlargement of flat display panels, such as PDP, ELD and dot matrix VFD, have been strongly demanded. Driver circuits for these display panels, necessarily have a lot of high voltage circuit outputs. Therefore, the monolithic IC equipped with high voltage transistors and their control logic circuits on the same chip, is essential to meet the above requirement. High voltage planar MOS ICs are thought to be most suited for such an IC, because of its isolation ease and high speed operation.[1]~[3]

However, negative resistance breakdown due to parasitic bipolar effect, is known to be observed in a high voltage planar NMOS transistor, a key device for high voltage MOS ICs.[4] Therefore, the high voltage transistor has a narrow ASO (Area of Safe Operation). To solve this problem, a high voltage MOS transistor with parasitic effect-free characteristic, was realized using the proposed "shielded source structure".[5][6]

The low voltage logic, for controlling the high voltage transistors, should be CMOS with low power dissipation and large noise immunity characteristic. However, since high resistivity substrate is used to realize high breakdown voltage for the high voltage MOS transistor, latch up phenomena in CMOS logic become easily to occur. Since the latch up is one of parasitic bipolar effect, the shielded source structure will be effective to suppress the latch up.

This paper describes, a newly developed, 16 output high voltage NMOS/CMOS logic IC without any parasitic effect. This is achieved by adopting shielded source structure. The possibility of realizing even higher integration density IC by using the shielded source structure is also discussed, based on experimental results.

## DEVICE STRUCTURE

In the new IC, the shielded source structure, in which the high impurity density $p^+$ ground layer entirely covers $n^+$ source layer except for the MOS channel plane, is adopted in high voltage NMOS transistors and in low voltage NMOS transistors for CMOS logic, as shown in Fig. 1. Since $p^+$ ground layer potential is equal to that for the source ($n^+$), even if voltage drop at the substrate due to substrate current occurs, the source junction is not forward-biased. In consequence, the parasitic bipolar effect doesn't occur. These $n^+$ source layer and underlying $p^+$ ground layer are simply fabricated by $As^+$ and $B^+$ ion implantations through the same source mask windows in a self-aligned manner.

The IC is made up of 8 input-output buffer circuits, 16 blocks of serial-in/parallel-out shift register, latch, gate and buffer circuit and 16 output high voltage NMOS transistors (Fig. 2). The buffer circuit consisting of 4 stage inverters is designed to have 5 MHz driving capability for the high voltage transistor gate. The high voltage transistors are controlled by Output Enable (OE), Toggle (To) and Data (D in1 or D in2) input signals. The CMOS logic includes about 700 low voltage MOS transistors.

## EXPERIMENTAL RESULTS

A photomicrograph of the IC is shown in Fig. 3. IC chip size is 6 mm x 6 mm. The IC electrical characteristics are shown in Table 1. High voltage NMOS transistors having 4 μm long, 10.2 mm wide MOS channel and 40 μm long offset gate, can flow 0.5 A drain current at 10 V gate bias, which is a high enough current level to drive a large display area dot matrix AC refresh PDP. The high voltage transistor shows about 400 V drain breakdown voltage in the 0 V to 15 V wide gate bias range without any negative resistance, according to pulse current-voltage measurement. This characteristic is still superior to that for 100-150 μm long offset gate conventional NMOS transistors. The conventional transistors have larger on-resistance and larger chip



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CH1973-7/83/0000-0416 $1.00 © 1983 IEEE

FCS1689187

occupation area compared to that for the shielded source transistor. Therefore, this structure enables easily realizing high integration density MOS ICs. Drain current-voltage characteristics for the high voltage shielded source transistor are shown in Fig. 4.

CMOS logic with shielded source structure (about 4 μm gate length) operates at 2-30 V power supply voltage range and follows 9 MHz clock frequency at 10 V (Fig. 5) (5-6 MHz clock frequency will be large enough for about 2000 character AC refresh PDP to be driven). CMOS logic power consumption is 21 mW at 10 V, 5 MHz clock frequency, which is much less than the power consumption for an E/D MOS logic (over 100 mW).

If integration density increases further, there is a possibility that logic error operation due to a capacitive coupling noise pulse would occur. By using CMOS configuration in logic, stable logic operation is expected to be obtained due to its large noise margin. The other possibility is that the interferences between high and high voltage transistors, high and low voltage transistors, and low and low voltage transistors due to a substrate current, would occur. The substrate current will be caused by low and high voltage transistor's avalanche phenomena, p-n junction's (for example, drain junction for CMOS logic) forward-biasing resulting from capacitive coupling noise pulse and surge voltage.

For example, a large quantity of electrons injected into the substrate diffuse to a certain high voltage transistor and are likely to lead this transistor to negative resistance breakdown by causing the parasitic bipolar transistor to turn on. To investigate such a parasitic bipolar effect, the following experiment was made. In a high voltage transistor biased at a lower voltage than its breakdown voltage, electrons are injected from an adjacent high voltage transistor's drain junction into the substrate, by forward-biasing. These electrons enter into the transistor drain depletion layer and cause avalanche breakdown. As a result, a large quantity of holes are injected into the substrate and cause voltage drop at the substrate. According to the experiment, a conventional transistor showed parasitic bipolar action in low injection current in spite of at lower electric field than that of breakdown, whereas the shielded source transistor didn't show negative resistance breakdown, even at experimentally observable 450 mA injection current level.

Also, there is a possibility that latch up might occur in CMOS logic due to the substrate current. Since high voltage MOS IC uses high resistivity substrate, parasitic lateral npn transistor's base resistance, or the substrate resistance, is high, as mentioned previously. Therefore, when the substrate current causes enough voltage drop at the substrate resistance to make n-channel transistor source junction forward-bias, latch up occurs. In order to investigate such a parasitic bipolar effect, CMOS ability to withstand latch up was experimented upon. The conventional CMOS with 20 μm parasitic lateral npn transistor base ($p^-$ substrate: $N_A = 6 \times 10^{14}$ $cm^{-3}$) width $L_M$, results in latch up phenomena, as shown in Fig. 6, at 6 mA parasitic vertical pnp transistor base (n-well region) injection current level, 10 V collector-emitter bias voltage. As compared with this characteristic, the CMOS with shielded source structure doesn't show latch up, even at 300-350 mA base injection current level. The reason is that current gain $\alpha_n$ for the parasitic npn transistor in the shielded source structure is less than $3 \times 10^{-7}$. These experimental investigations show that higher integration density IC will be realized.

The fabricated ICs in 28 pin ceramic packages were applied in a plasma display scan driver. The ICs successfully drove the panel at 200 V, 2 MHz without any parasitic effect and any logic operation error due to a capacitive coupling noise pulse (Fig. 7). As a result, in a practically usable high voltage IC, since parasitic bipolar action was effectively suppressed by using the shielded source structure, the high IC reliability was confirmed.

## CONCLUSION

A 16 output high voltage NMOS/CMOS logic IC, designed for driving an AC refresh PDP, was developed using shielded source structure for its NMOS tansistors, to realize completely parasitic effect-free high voltage MOS ICs.

Practically, the IC succeeded in driving an AC refresh PDP and its high reliability was verified.

Parasitic effects due to the interferences between high and high voltage transistors, low and high voltage transistors, and low and low voltage transistors in this IC, were experimentally investigated.

These results indicate that much higher packing density, but still a parasitic effect-free high voltage NMOS/CMOS logic IC, will be realized using shielded source structure.

## ACKNOWLEDGEMENT

The authors wish to thank Drs. K. Ayaki and H. Kato for their continuous encouragement and T. Aizawa and K. Hirata for their technical assistance.

## REFERENCES

[1] K. Fujii et al., "400 V MOS IC for EL Display," ISSCC Digest of Technical Papers, p.46, Feb., 1981.
[2] S.A. Buhler et al., "Integrated High-Voltage/Low-Voltage MOS Devices," IEDM Technical Digest, p.259, Dec., 1981.
[3] B. Weir, "Integrated High-Votlage Driver Circuits in Gate Array Form," SID 1982 Digest, p.268.
[4] I. Yoshida et al., "Thermal Stability and Secondary Breakdown in Planar Power MOSFET's," IE$^3$ ED, Vol. ED-27, No.2, p.395, Feb., 1980.
[5] H. Sakuma et al., "Parasitic Effect-Free, High Voltage MOS ICs with Shielded Source Structure," IEDM Technical Digest, p.254, Dec., 1982.
[6] H. Sakuma et al., "Parasitic Effect Free, High Voltage NMOS/CMOS Logic ICs with Shielded Source Structure," Technical Report of IECE, ED 83-8, Apr., 1983.

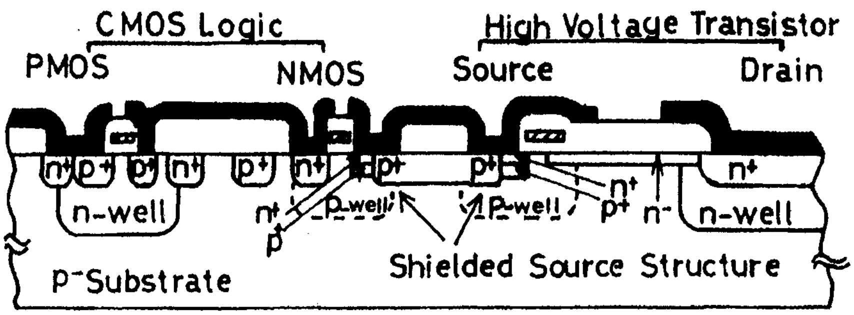



Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper $n^+$ source layer entirely shielded by a lower $p^+$ ground layer.

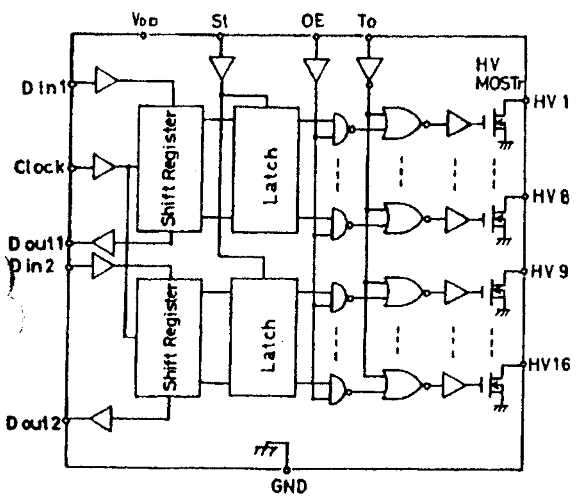



Fig.2 16 output high voltage MOS IC blockdiagram. Logic circuit is composed of serial-in and parallel-out shift registers, latches, gates and buffers.

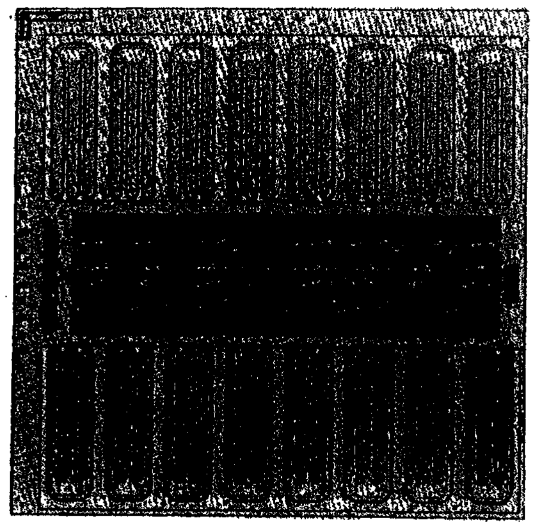


Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

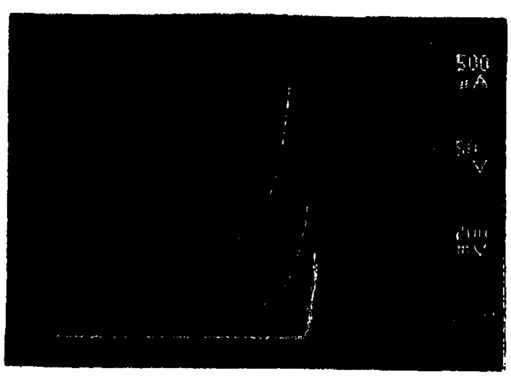


Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

| High Voltage MOS Tr | |
|---|---|
| $BV_{DSS}$ (at $I_D$<100 μA) | 400 V |
| Ron (at $V_G$=10 V) | 30 Ω |
| $I_{DS}$ (at $V_G$=10 V) | 0.5 A |
| **Low Voltage Logic Circuit** | |
| $f_{clock}$ max (at $V_{DD}$=10 V) | 9 MHz |
| $V_{DD}$ | 2V～30 V |
| $P_o$ (at $V_{DD}$=10V, $f_{clock}$=5MHz, $C_L$=15pF) | 21 mw |

Table 1 Typical 16 output high voltage MOS IC characteristics. CMOS logic circuit can operate in wide power supply voltage range. High voltage NMOS transistor doesn't show any parasitic bipolar effect for wide gate bias range from 0 V to 15 V.

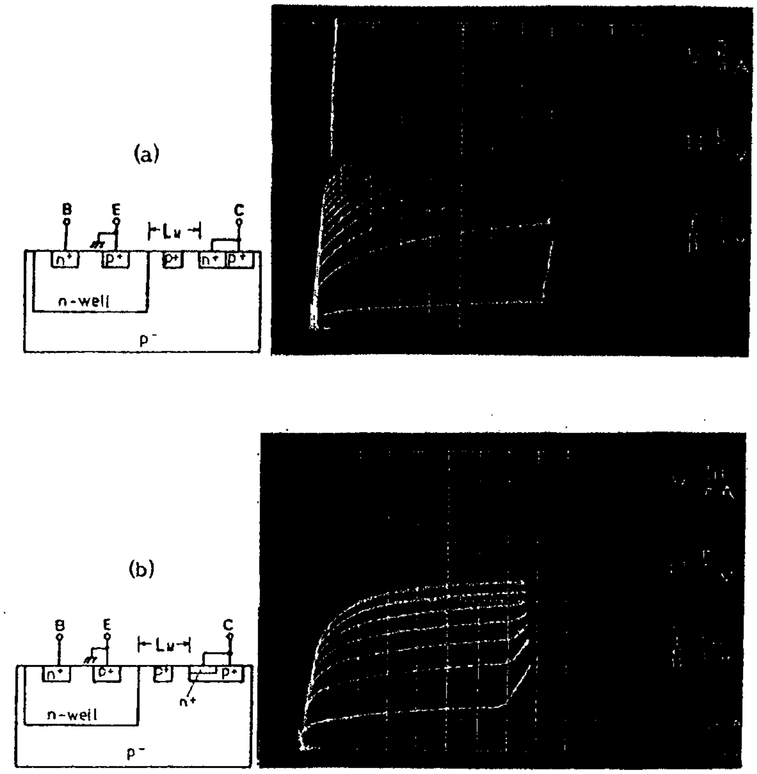



Fig.6 Base noise current at latch up. (a) For conventional CMOS. (b) For CMOS with shielded source structure. Conventional CMOS shows latch up at 6 mA base injection current level, 10 V collector-emitter bias voltage, whereas CMOS with shielded source structure doesn't show latch up phenomena, even at 350-400 mA.

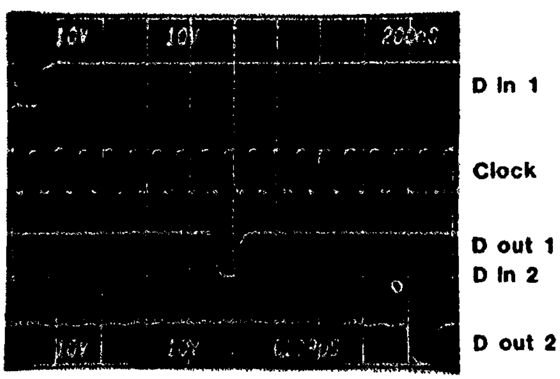



Fig.5 16 stage shift register's input and output waveforms at 9 MHz clock frequency, 10 V. Shift registers operate up to 12 MHz, at 20 V.

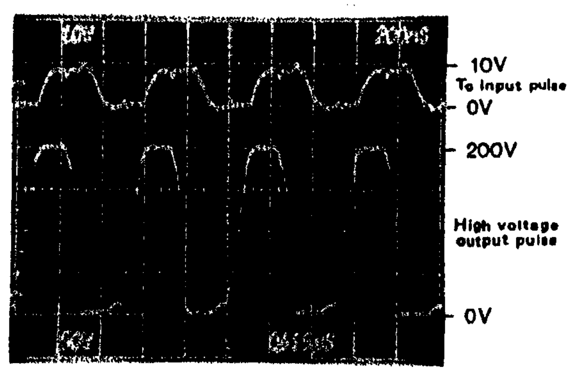
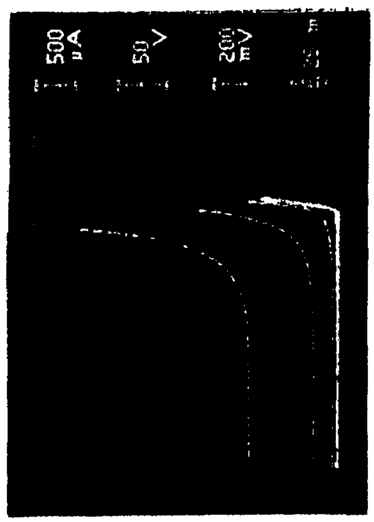
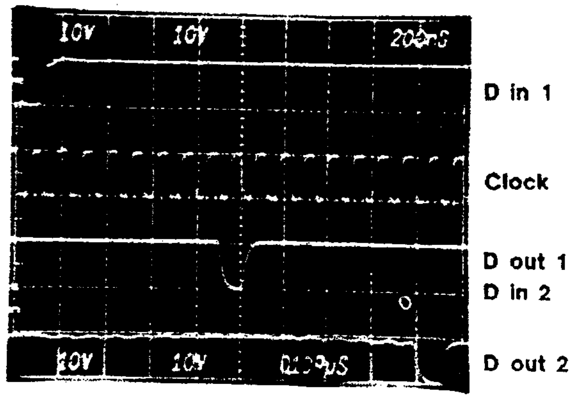



Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.



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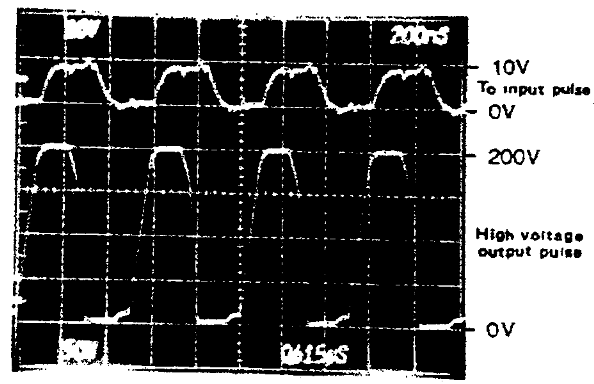


Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.

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